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Notice of Allowability	Application No.	Applicant(s)	
	10/664,384	AUGSBURG ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 26 June 2007*.

2. ☒ The allowed claim(s) is/are *1-3, 5-7, 16-18, 20-23, 31, 34-36, and 38-40 renumbered as 1-3, 4-6, 7-9, 10-13, 14, 15-17, and 18-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with James O. Skarsten (Reg. No. 28,346) on 14 September 2007.

3. The application has been amended as follows:

a. Claim 1:

i. A method for issuing instructions in a multithreaded computer processor, the method comprising the steps of:

(1) Receiving a set of computer instructions in an instruction issue logic, wherein each instruction of said set comprises one instruction from each of a plurality of independent instruction threads;

(2) Identifying as dependent instructions those received instructions that require a result from a prerequisite instruction;

(3) Determining a probability for each received instruction that the **received** instruction will complete all stages of a multi-stage instruction pipeline of the processor without causing a stall, wherein the probability for each received instruction is expressed as a percentage value;

(4) Selecting the received instruction of the set that is least likely to cause a stall in the multi-stage pipeline; and

(5) Issuing-the selected instruction into the pipeline for processing, from the instruction issue logic, when the probability for the selected instruction is above a predetermined threshold that is 50%.

b. Claim 5

i. The method of claim 1, further comprising: predicting a stage, within the multi-stage instruction pipeline, where results of each instruction will be available, and said step of determining the probability for a received instruction includes calculating a critical distance comprising **[[the]]a** number of stages between a stage when the **received** instruction will need a given result, and **[[the]]a** stage when the result will be available.

c. Claim 6

i. The method of claim 5, wherein the probability for a dependent instruction is determined based upon **[[the]]a** current location and **[[the]]a** predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

d. Claim 7

i. The method of claim 6, further comprising the step of dynamically recalculating the probability for each instruction based on **[[the]]**current contents of the pipeline and a current status of any shared resources.

e. Claim 16

i. A simultaneous multithreaded computer processor with speculative instruction issue that increases throughput, the computer processor comprising:

(1) Multiple independent input buffers, wherein one set of buffers is provided for each of a plurality of independent threads of instructions;

(2) Instruction issue logic that has an output buffer and is connected to the independent input buffers, wherein the instruction issue logic:

(a) Receives a set of instructions comprising one instruction from each of the threads of instructions;

(b) Identifies as dependent instructions those received instructions that require a result from a prerequisite instruction;

(c) Determines a probability for each instruction that the **each** instruction will complete all stages of a multi-stage instruction pipeline of the processor without causing a stall, wherein the probability for each received instruction is expressed as a percentage value;

(d) Selects the received instruction of the set that is least likely to cause a stall in the multistage pipeline; and

(e) Issues the selected instruction into the pipeline for processing, from the instruction issue logic, when the

probability for the selected instruction is above a predetermined threshold that is 50%; and

(f) Wherein a first stage of the multi-stage pipeline is connected to an output buffer of the instruction issue logic.

f. Claim 18

i. The computer processor of claim **[[16]]17**, wherein the instruction issue logic resolves a given one of said shared resource conflicts, between two or more of said received instructions, after said given conflict has been discovered.

g. Claim 20

i. The computer processor of claim 16, wherein the instruction issue logic predicts a stage, within the multi-stage instruction pipeline, where results of each instruction will be available, and determines the probability for a dependent instruction by calculating a critical distance comprising **[[the]]a** number of stages between a stage when the dependent instruction will need a given result, and **[[the]]a** stage when the result will be available.

h. Claim 22

i. The computer processor of claim 21, wherein the probability for a dependent instruction is determined based upon a current location and **[[the]]a** predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

i. Claim 31

i. A method for issuing instructions in a multithreaded computer processor, comprising the steps of:

(1) Receiving a set of computer instructions in an instruction issue logic, wherein each set of instructions comprises one instruction from each of a plurality of independent instruction threads;

(2) Predicting a stage, within a multi-stage instruction pipeline of the computer processor, where results of each instruction will be available;

(3) Identifying as dependent instructions those received instructions that require a result from a prerequisite instruction;

(4) Calculating a critical distance comprising **[[the]]a** number of stages between a stage when a selected dependent instruction will need a given result, and **[[the]]a** stage when the result will be available;

(5) Determining whether the selected instruction is within **[[the]]a** critical distance, and if so, determining a probability that the selected instruction will complete all stages of the pipeline without causing a stall, wherein said probability is expressed as a percentage value; and,

(6) Issuing the selected instruction into the pipeline for processing, from the instruction issue logic, when the probability is above a predetermined threshold that is 50%.

j. Claim 38

i. The computer program product of claim 34, further comprising: seventh instructions for predicting a stage, within the multi-stage instruction pipeline, where results of each instruction will be available, and determining a probability for a received instruction by calculating a critical distance comprising **[[the]]a** number of stages between a stage when the **received** instruction will need a given result, and **[[the]]a** stage when the result will be available.

k. Claim 39

i. The computer program product of claim 38, wherein the probability for a dependent instruction is determined based upon **[[the]]a** current location and **[[the]]a** predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

REASONS FOR ALLOWANCE

4. The following is an examiner's statement of reasons for allowance: The amended claims recite the limitations

> Determining a probability for each received instruction that the instruction will complete all stages of a multi-stage instruction pipeline of the processor without causing a stall, wherein the probability for each received instruction is expressed as a percentage value...
>
> ...

Issuing the selected instruction into the pipeline for processing, from the instruction issue logic, when the probability for the selected instruction is above a predetermined threshold that is 50%."

5. As stated in the previous Office Action, most prior art searched and found have taught that the possibility of a data dependency is either 100%, i.e. that a data dependency definitely exists, or 0%, i.e. that a data dependency definitely does not exist. None of the prior art has taught that the threshold value being tested is between 0% and 100%, i.e. that the data dependency is 100% certain or 0% certain. The small amounts of prior art that did discuss finding confidence values did not discuss these values being definitive, quantitative values, such as percentages, but that they are possibilities with more qualitative values, such as stronger to weaker likelihoods.

6. Also, in the broader sense, the probability of a dependency is similar to confidence values commonly used in branch prediction. However, the prior art associated with confidence values does not teach or even suggest that the confidence values are expressed as percentage values, specifically a percentage value of 50%. Rather, the most common expression of confidence values are as counters that increment one bit when a prediction is true and decrement when a prediction is false. This means that the confidence values are expressed by a combination of bits, not a percentage, and the combination of bits typically represent a more broad qualitative value, such as strongly not-taken, not-taken, taken, and strongly taken, not a specific quantitative value, such as 50%.

Conclusion

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J. Li

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Examiner
Art Unit 2183

13 September 2007